Test cases

\*Assuming a clock period of 10

|  |  |  |
| --- | --- | --- |
| Design | Timing Report Without Setting Wire\_RC | Timing Report With after Setting Wire\_RC layer1 |
| Crc32 | 7.16 | 7.11 |
| Spi\_master | 3.57 | 3.55 |
| Rle\_enc | 7.47 | 7.45 |
| Uart | 6.87 | 6.83 |
| Cpu | 2.84 | 2.77 |